REMARKS

Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004). Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian and in view of Yu et al (U.S. Patent No. 6,225,167). Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian. Claims 9-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. Patent No. 6,225,167B1) in view of Balasubramanian. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian and Yu in view of Hayakawa (U.S.Patent No. 5,779,520).

1. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 1-17 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in specification, Paper No.1, filed March 25, 2002. In that paper, applicant has stated "contaminants adhering to the semiconductor wafer 100 **are removed**"(see [0025]); "the present invention shows marked improvement in **preventing the occurrence of particles and defects** of various shapes and sizes" (see [0030]), and this statement indicates that the invention is different from what is defined in the claims(s) because claim 2 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (line 2) and "which **utilizes the particles** on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the

polysilicon film"(line 10-12).

Note that, "preventing the occurrence of particles and defects" is achieved by the cleaning process, not the formation of the α-Si.

With respect to claim 4, claim recites: "wherein the wet etching process comprises a megasonic scrubbing process, a SC-1 cleaning process and a SC-2 cleaning process".

However, the specification discloses: "After removing the photoresist layer 112, a wet etching process is performed. Usually, a megasonic scrubbing process is first performed. By utilizing vibration of the megasonic scrubbing, contaminants, adhereing to the semiconductor wafer 100 **are removed**". (See [0025]).

As disclosed, the megasonic scrubbing is **not** part of the wet etching but is part of the cleaning process. While the wet etch is to remove the oxide formed in the area 104. (See Fig.10, also see claim 13).

Response:

In the above AMENDMENTS TO THE CLAIMS section, the term "which utilizes the particles on the surface of the semiconductor wafer" in claim 1 is changed to "which growing by way of the particles on the surface of the semiconductor wafer". The amended portion is disclosed in the specification on page 7, lines 18-21. No new matter is included.

In claim 4, the term "wet etching process" is changed to "wet cleaning process" in the above AMENDMENTS TO THE CLAIMS section, and the terms "a wet etching process" in Page 2, line 33 and Page 6, line 19 of the specification are changed to "a wet cleaning process" in the above AMENDMENTS TO THE SPECIFICATION section due to editorial errors.

Please refer to the response to the rejection over claims 1,7, and 8 under 35 U.S.C. 102(b) (item 4) for the reason that "preventing the occurrence of particles and defects" is achieved by the formation of the α-Si, not the cleaning process. Reconsideration of the rejection over claims 1-17 is hereby requested.

2. Claims 1-17 are rejected under 35 U.S.C., second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites: "the surface of the semiconductor wafer **comprising a plurality of particles**" (line 2) and "which **utilizes the particles** on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film" (line 10-12).

Limitation of claim 1 are inconsistent with the aim of the present invention, e.g. preventing the occurrence of particles and defects.

The specification clearly states "Consequently, grains growing via small and large particles adhering on the surface of the semiconductor wafer during the crystallization, and which thus generate various unexpected needle-like particles, **can be avoided**". (See[0030]).

With respect to claim 9, the "avoid formation of particles and defects" are the result of the cleaning process, not the deposition process.

The indefiniteness of claim 5 and 17, have prevented these claims from being properly examined for merits.

Response:

In the above AMENDMENTS TO THE CLAIMS section, the term "which utilizes the particles on the surface of the semiconductor wafer" in claim 1 is changed to "which growing by way of the particles on the surface of the semiconductor wafer", and the term "a first step low temperature amorphous silicon (α -Si) deposition process to avoid formation of particles and defects during the formation of the polysilicon layer" in claim 9 is changed to "a first step low temperature amorphous silicon (α -Si) deposition process to avoid formation of particles and defects by inhibiting nucleation during the formation of the polysilicon layer". The amended portion is disclosed in the specification on page 7, lines 18-21. No new matter is included.

In claims 5, the term particle means the already existing particles on the surface of the semiconductor wafer before performing the two-step silicon deposition process. In claim 17, the term particles means the needle-like defects formed after the two-step silicon deposition process.

Please refer to the response to the rejection over claims 1,7, and 8 under 35 U.S.C. 102(b) (item 4) for the reason that "preventing the occurrence of particles and defects" is achieved by the formation of the α -Si, not the cleaning process. Reconsideration of the rejection over claims 1-17 is hereby requested.

3. Claims 1,8,9 and 16 are objected to because of the following informalities:

Claim 1 recites: "performing a <u>two-step polysilicon</u> deposition process", the correct terminology should be

"performing a two-step **silicon** deposition process" because layer 116a is **amorphous** silicon, not polysilicon.

Appropriate correction is required.

Response:

In the above AMENDMENTS TO THE CLAIMS section, the terms "two-step polysilicon deposition process" in claims 1,8,9,and 16 are changed to "two-step silicon deposition process" as requested by the examiner. In addition, the term "two-step polysilicon deposition process" in claim 2 is changed to "two-step silicon deposition process" for consistency. No new matter is included. Reconsideration of the rejection over claims 1,8,9,and 16 is hereby requested.

4. Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Balasubramanian et al. (U.S. Patent No. 5,767,004).

With respect to claim 1, as best understood by the examiner, Balasubramanian teaches a method for making a polysilicon film on a semiconductor wafer, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (16) deposition process utilizing a low temperature; and

a second step polysilicon (18) deposition process utilizing high temperature;

wherein the first step amorphous silicon (16) deposition process is used to avoid nucleation of the polysilicon film growth, so as to inhibit occurrences of needlelike particles and defects on the surface of the polysilicon film. (See Fig.1, col.1-12).

With respect to claim 7, the polysilicon layer (18) of

Balasubramanian is deposited at the temperature that includes the claimed range.

With respect to claim 8, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian includes single wafer type LPCVD equipment.

Response:

First, claim 1 is amended in the above AMENDMENTS TO THE CLAIMS section to overcome this rejection and the newly added portion is disclosed in the specification on page 7, lines 18-21. No new matter is introduced.

Second, the Applicant intends to point out the difference between the amended claim 1 of the present application and Balasubramanian's disclosure. The amended claim 1 of the present application is repeated below:

1. (Currently amended) A method for making a polysilicon film on a semiconductor wafer, the surface of the semiconductor wafer comprising a plurality of particles, the method comprising:

performing a two-step silicon deposition process, the two-step silicon deposition process comprising:

a first step amorphous silicon (α -Si) deposition process utilizing a low temperature; and

a second step polysilicon deposition process utilizing a high temperature;

wherein **the first step amorphous silicon (α -Si) deposition**

process is used to avoid nucleation of the polysilicon film growth, which growing by way of the particles on the surface of the semiconductor wafer, so as to inhibit occurrences of needle-like particles and defects on the surface of the polysilicon film.

As disclosed in the amended claim 1 of the present application, there is one obvious difference between Balasubramanian's invention and the present application. According to Balasubramanian's invention, an anneal process is taught to form a low impurity diffusion polysilicon layer. By **simultaneously performing the annealing process to a formed amorphous silicon layer and a polysilicon layer, a polysilicon multi-layer with grain boundary mis-matched polycrystalline properties is formed.** With the grain boundary mis-matched polycrystalline properties, inter-diffusion of impurities are inhibited to result in the low impurity diffusion polysilicon layer. **In other words, Balasubramanian never teaches how to form a polysilicon layer by only utilizing a two-step silicon deposition process.** Rather, an annealing process is necessary in Balasubramanian's invention.

In addition, Balasubramanian **never teaches how to utilize a first step amorphous silicon deposition process to inhibit occurrences of needle-like particles and defects** on the surface of the final formed polysilicon film. In the present application, **even though originally the surface of the semiconductor wafer comprises a plurality of particles**, the occurrences of needle-like particles and defects on the surface of the

final formed polysilicon film are inhibited **because the first step amorphous silicon deposition process can avoid nucleation of the polysilicon film growth by way of the particles on the surface of the semiconductor wafer**. Therefore, "preventing the occurrence of particles and defects" is achieved by the first step amorphous silicon deposition process, not by the cleaning process.

From the above discussion, the Applicant believes that the amended claim 1 of the present application is absolutely different from Balasubramanian's disclosure. Reconsideration of the rejection over the amended claim 1 is hereby requested.

As claims 7-8 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the rejection over claims 7-8 is therefore requested.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian "004 as applied to claim 1 above, and further inview of Yu et al. (U.S. Patent No.6,225,167).

With respect to claim 2, Balasubramanian teaches a method of making a polysilicon film on a semiconductor wafer including performing a two-step silicon deposition process.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of disclosing the process performing before the two-step silicon deposition process.

However, Yu teaches the process performing prior to making conductive gate electrodes including: at least one photolithography process, one wet etching process, one

photoresist stripping process, one wet cleaning process and one thermal oxidation process are performed on the surface of the semiconductor wafer(200).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to before performing the two-step silicon deposition process of Balasubramanian performing the processes as tqught by Yu to form the gate oxide for the silicon gate electrodes,

With respect to claim 3, as best understood by the examiner, the wet etching process of Yu comprises a buffer oxide etchant (BOE) etching process and followed by SC-1 cleaning process.

Response:

As claims 2-3 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the rejection over claims 2-3 is therefore requested.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004.

Balasubramanian teaches the first step amorphous (16) is deposited at a temperature range that overlaps the claimed range and at a thickness of about 400Å.

Thus, Balasubramanian is shown to teach all the features of the claim with the exception of explicitly forming a thinner amorphous layer. Note that, the claimed thickness does not appear to be critical.

Therefore, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum thickness of the amorphous silicon layer in the formation of the conductive gate electrodes. See In re Aller, Lacey and Hall (10 USPQ 233-237)"It is not inventive to discover optimum

or workable ranges by routine experimentation".

Response:

As claim 6 is dependent upon the amended claim 1, it should be allowed if the amended claim 1 is allowed. Reconsideration of the rejection over claim 6 is therefore requested.

7. Claims 9-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu '167 in view of Balasubramanian '004.

Yu teaches a method for forming a polysilicon film on a semiconductor wafer, a surface of the semiconductor wafer comprising a first gate oxide area (40) and a second gate oxide area (50), substantially as claimed including:

forming a first gate oxide layer (20) on the surface of the semiconductor wafer (10);

performing a photolithography process and an etching process to remove the first gate oxide layer (20) on the surface of the second gate oxide area (50);

performing a cleaning process; and performing a conductive gate electrodes deposition process covering he first gate oxide area (40) and the second gate oxide area (50) to form MOS transistors. (See Fig.1a-d, col. 1-10).

Thus, Yu is shown to teach all the features of the claim with the exception of explicitly disclosing process of making the conductive gate electrodes.

However, Balasubramanian teaches a process of forming conductive gate electrodes covering gate oxide including:

performing a two-step silicon deposition process to form a polysilicon layer (18), the polysilicon layer (18) covering the gate oxide layer (14);

wherein the two-step silicon deposition process comprises

a first step low temperature amorphous silicon (16) deposition process to avoid formation of particles and defects during the formation of the polysilicon layer (18), and a second step high temperature polysilicon (18) deposition process. (See Fig.1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the conductive gate electrodes of Yu using the two-step silicon deposition process as taught by Balasubramanian to form a low impurity diffusion polysilicon layer within an integrated circuit. (See col.3, lines 6-8).

With respect to claim 10, the etching process of Yu is a wet etching process.

With respect to claim 11, the wet etching process utilizes a buffer oxide etchant(BOE).

With respect to claim 12, the cleaning process of Yu is a wet etching process.

With respect to claims 14 and 15,the temperature ranges of the first step low temperature of amorphous silicon (16) deposition process and second step high temperature polysilicon (18) deposition process of Balasubramanian overlaps the claimed range.

With respect to claim 16, the two-step silicon deposition process of Balasubramanian is performed in single wafer type LPCVD equipment.

Note that, until proven otherwise, the LPCVD equipment of Balasubramanian ncludes single wafer type LPCVD equipment.

Response:

From the response to the rejection over Claims 1, 7 and 8 under 35 U.S.C. 102(b)(item 4), the Applicant believes that the amended claim 9 of the present application is absolutely

different from the combination technique of Yu's disclosure and Balasubramanian's disclosure. Reconsideration of the rejection over the amended claim 9 is hereby requested.

As claims 10-12 and 14-16 are dependent upon the amended claim 9, they should be allowed if the amended claim 9 is allowed. Reconsideration of the rejection over claims 10-12 and 14-16 is therefore requested.

8. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balasubramanian '004 and Yu '167 as applied to claims 2 and 9 above, and further in view of Hayakawa (U.S. Patent No. 5,779,520).

As best understood by the examiner, Balasubramanian '004 and Yu '167 teach a wet cleaning process utilizing RCA clean. Note that RCA cleaning comprises SC-1 and SC-2.

Thus, Balasubramanian '004 and Yu '167 are shown to teach all the features of the claim with the exception of further utilizing megasonic scrubbing.

However, Hayakawa teaches: cleaning is more effective with physical scrubbing including megasonic scrubbing (See col.2, lines 56-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to combine RCA cleaning of Yu with megasonic scrubbing as taught by Hayakawa for utmost effective in removing contaminants.

Response:

As claim 4 and claim 13 is dependent upon the amended claim 1 and the amended claim 9 respectively, they should be allowed if the amended claim 1 and the amended claim 9 are allowed. Reconsideration of the rejection over claim 4 and claim 13

is therefore requested.

Sincerely yours,

Winston Hsu Date: 7/4/2003

Winston Hsu, Patent Agent No.41,526
P.O. Box 506
Merrifield, VA 22116
U.S.A.
e-mail:winstonhsu@naipo.com.tw